Low Power Memory Compiler
Single Port SRAM
GF 22nm FDX®

SILVACO

Overview

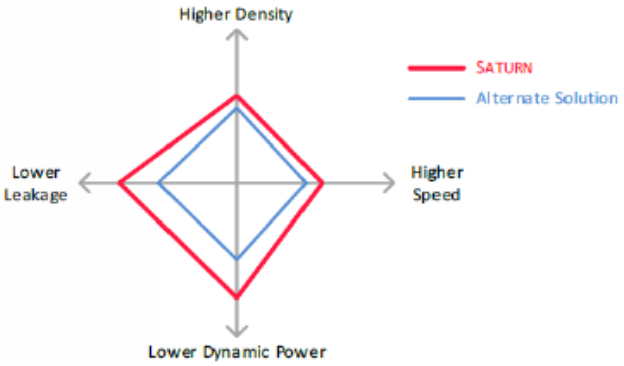
Natively designed to be ultra-low power, this memory leverages body biasing to reduce static power consumption, meeting the stringent power requirements of IoT, BLE, and automotive applications.

Highlights

- **Optimized power supply solution**
  - o Active usage of body bias to achieve optimal power and performance
  - o Dual rail operation
  - o Logic: 0.65 V +/-10% or 0.8 V +/-10%
  - o Array: 0.8 V +/-10%
- **FD-SOI optimized**
  - o Tunable performance: power/speed optimization through adaptive or pre-set body biasing
  - o Leakage is lowered due to insulator layer
  - o Lower variability across die due to lower doping effort
- **Optimized Architecture**
  - o Several low power modes for optimized saving
- **Flexible integration**
  - o Fully functional without Body Biasing
  - o Compatible with any Body Biasing generator
- **Other Features**
  - o Embedded retention and shut-down switches
  - o Variable Write Mask

Applications

The Saturn Advantage

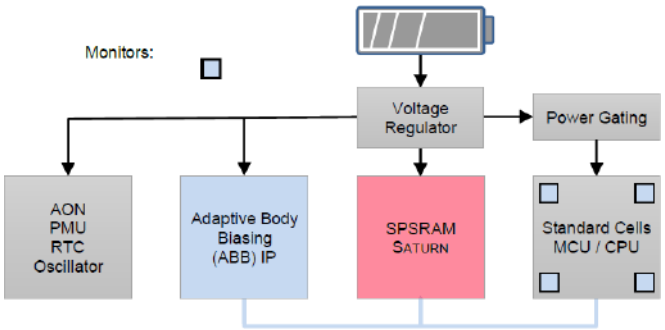


Compiler Specifications

Mux	Address Range	Address Increment Step	Word Width (bits)	Word Width Increment
4	32k - 4k	32	4- 256	1

Energy Efficient Solution for GF 22nm FDX®

- Compatible with Industry Adaptive Body Biasing IP
- Body Biasing functionality (-2.0 V /+2.0 V) to reduce leakage at the same supply level
- Part of the Silvaco GF 22nm FDX®-PLUS IP portfolio



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